

## CD4094BC 8-Bit Shift Register/Latch with 3-STATE Outputs

### General Description

The CD4094BC consists of an 8-bit shift register and a 3-STATE 8-bit latch. Data is shifted serially through the shift register on the positive transition of the clock. The output of the last stage ( $Q_8$ ) can be used to cascade several devices. Data on the  $Q_8$  output is transferred to a second output,  $Q'_8$ , on the following negative clock edge.

The output of each stage of the shift register feeds a latch, which latches data on the negative edge of the STROBE input. When STROBE is HIGH, data propagates through

the latch to 3-STATE output gates. These gates are enabled when OUTPUT ENABLE is taken HIGH.

### Features

- Wide supply voltage range: 3.0V to 18V
- High noise immunity:  $0.45 V_{DD}$  (typ.)
- Low power TTL compatibility:
  - Fan out of 2 driving 74L or 1 driving 74LS
- 3-STATE outputs

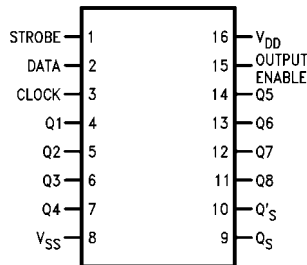
### Ordering Code:

Order Number	Package Number	Package Description
CD4094BCWMM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
CD4094BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram

Pin Assignments for DIP and SOIC



### Truth Table

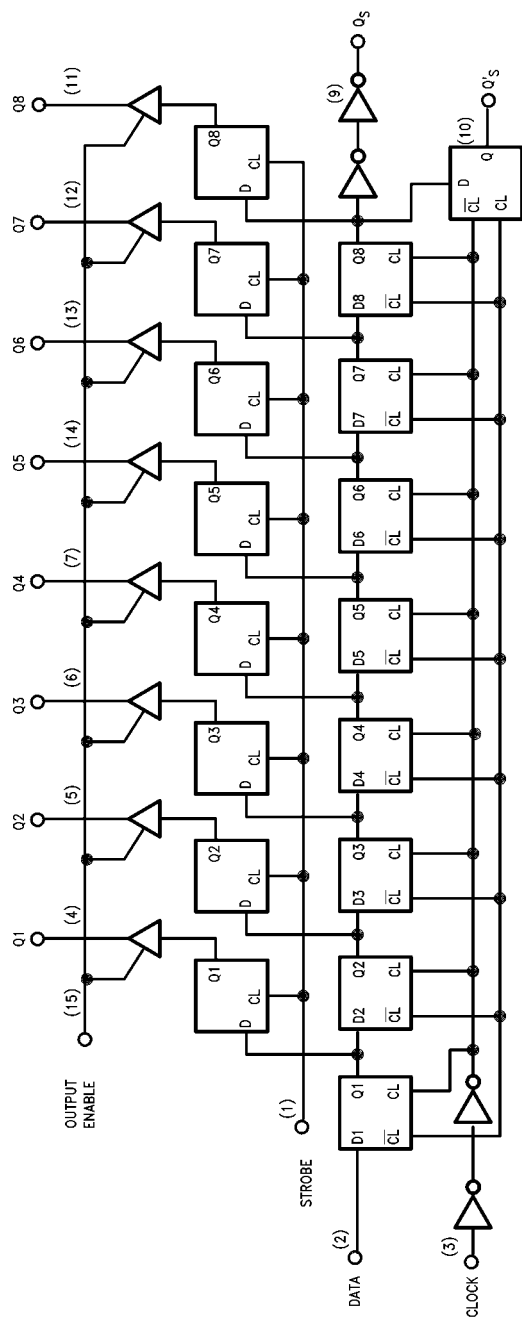
Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q <sub>N</sub>	Q <sub>S</sub> (Note 1)	Q' <sub>Σ</sub>
↘	0	X	X	Hi-Z	Hi-Z	Q7	No Change
↙	0	X	X	Hi-Z	Hi-Z	No Change	Q7
↘	1	0	X	No Change	No Change	Q7	No Change
↘	1	1	0	0	Q <sub>N-1</sub>	Q7	No Change
↘	1	1	1	1	Q <sub>N-1</sub>	Q7	No Change
↙	1	1	1	No Change	No Change	No Change	Q7

X = Don't Care  
↘ = HIGH-to-LOW  
↙ = LOW-to-HIGH

**Note 1:** At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q<sub>S</sub>.

CD4094BC

Block Diagram



<b>Absolute Maximum Ratings</b> (Note 2)		<b>Recommended Operating Conditions</b> (Note 3)	
(Note 3)			
Supply Voltage ( $V_{DD}$ )	-0.5 to +18 $V_{DC}$	DC Supply Voltage ( $V_{DD}$ )	+3.0 to +15 $V_{DC}$
Input Voltage ( $V_{IN}$ )	-0.5 to $V_{DD} + 0.5 V_{DC}$	Input Voltage ( $V_{IN}$ )	0 to $V_{DD} V_{DC}$
Storage Temperature Range ( $T_S$ )	-65°C to +150°C	Operating Temperature Range ( $T_A$ )	-40°C to +85°C
Power Dissipation ( $P_D$ )		<b>Note 2:</b> "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.	
Dual-In-Line	700 mW	<b>Note 3:</b> $V_{SS} = 0V$ unless otherwise specified.	
Small Outline	500 mW		
Lead Temperature ( $T_L$ )			
(Soldering, 10 seconds)	260°C		

**DC Electrical Characteristics** (Note 3)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5.0V$		20			20		150	$\mu A$
		$V_{DD} = 10V$		40			40		300	$\mu A$
		$V_{DD} = 15V$		80			80		600	$\mu A$
$V_{OL}$	LOW Level Output Voltage	$V_{DD} = 5.0V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$	$ I_O  \leq 1.0 \mu A$	0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
$V_{OH}$	HIGH Level Output Voltage	$V_{DD} = 5.0V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10.0		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15.0		14.95		V
$V_{IL}$	LOW Level Input Voltage	$V_{DD} = 5.0V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
$V_{IH}$	HIGH Level Input Voltage	$V_{DD} = 5.0V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
$I_{OL}$	LOW Level Output Current (Note 4)	$V_{DD} = 5.0V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
$I_{OH}$	HIGH Level Output Current (Note 4)	$V_{DD} = 5.0V, V_O = 4.6V$	-0.52		-0.44	0.88		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.3		-1.1	2.25		-0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	-3.6		-3.0	8.8		-2.4		mA
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.3			-0.3		-1.0	$\mu A$
		$V_{DD} = 15V, V_{IN} = 15V$		0.3			0.3		1.0	$\mu A$
$I_{OZ}$	3-STATE Output Leakage Current	$V_{DD} = 15V, V_{IN} = 0V$ or $15V$		1			1		10	$\mu A$

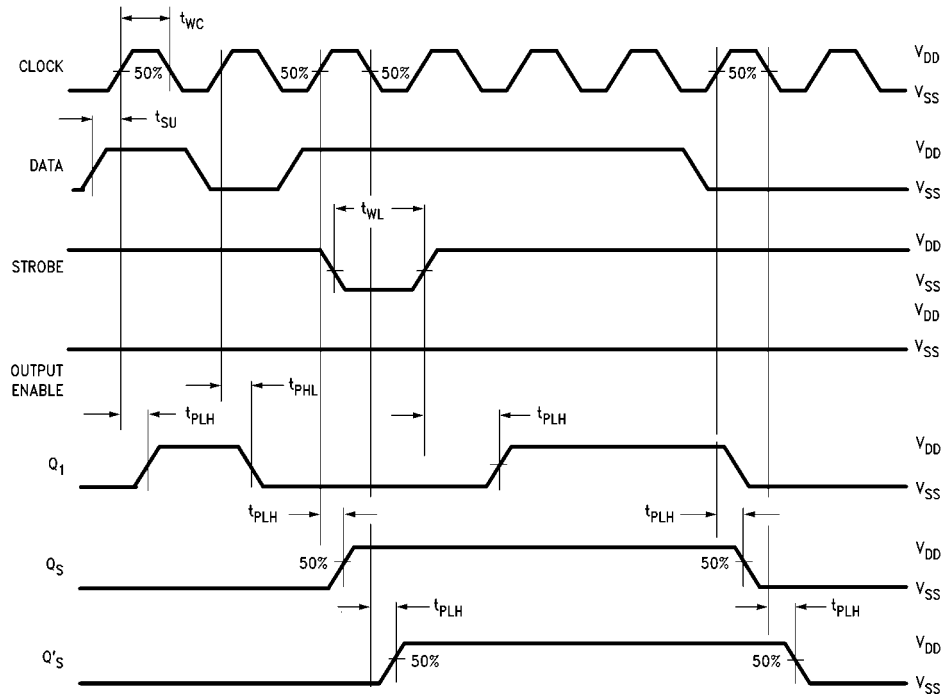
**Note 4:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

**AC Electrical Characteristics** (Note 5)T<sub>A</sub> = 25°C, C<sub>L</sub> = 50 pF

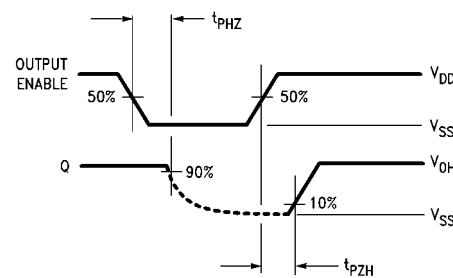
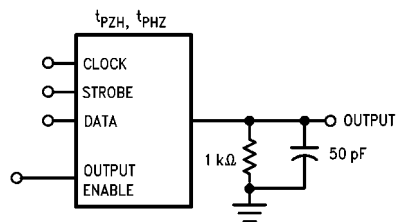
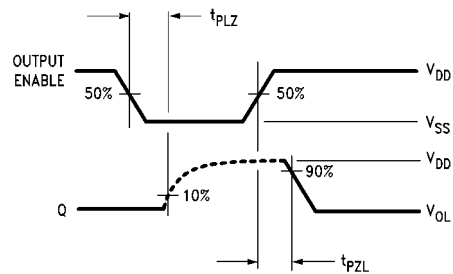
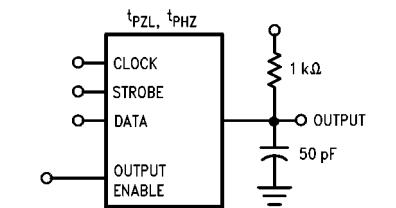
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Clock to Q <sub>S</sub>	V <sub>DD</sub> = 5.0V		300	600	ns
		V <sub>DD</sub> = 10V		125	250	ns
		V <sub>DD</sub> = 15V		95	190	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Clock to Q' <sub>Σ</sub>	V <sub>DD</sub> = 5.0V		230	460	ns
		V <sub>DD</sub> = 10V		110	220	ns
		V <sub>DD</sub> = 15V		75	150	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Clock to Parallel Out	V <sub>DD</sub> = 5.0V		420	840	ns
		V <sub>DD</sub> = 10V		195	390	ns
		V <sub>DD</sub> = 15V		135	270	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Strobe to Parallel Out	V <sub>DD</sub> = 5.0V		290	580	ns
		V <sub>DD</sub> = 10V		145	290	ns
		V <sub>DD</sub> = 15V		100	200	ns
t <sub>PHZ</sub>	Propagation Delay HIGH Level to HIGH Impedance	V <sub>DD</sub> = 5.0V		140	280	ns
		V <sub>DD</sub> = 10V		75	150	ns
		V <sub>DD</sub> = 15V		55	110	ns
t <sub>PLZ</sub>	Propagation Delay LOW Level to HIGH Impedance	V <sub>DD</sub> = 5.0V		140	280	ns
		V <sub>DD</sub> = 10V		75	150	ns
		V <sub>DD</sub> = 15V		55	110	ns
t <sub>PZH</sub>	Propagation Delay HIGH Impedance to HIGH Level	V <sub>DD</sub> = 5.0V		140	280	ns
		V <sub>DD</sub> = 10V		75	150	ns
		V <sub>DD</sub> = 15V		55	110	ns
t <sub>PZL</sub>	Propagation Delay HIGH Impedance to LOW Level	V <sub>DD</sub> = 5.0V		140	280	ns
		V <sub>DD</sub> = 10V		75	150	ns
		V <sub>DD</sub> = 15V		55	110	ns
t <sub>THL</sub> , t <sub>TLH</sub>	Transition Time	V <sub>DD</sub> = 5.0V		100	200	ns
		V <sub>DD</sub> = 10V		50	100	ns
		V <sub>DD</sub> = 15V		40	80	ns
t <sub>SU</sub>	Set-Up Time Data to Clock	V <sub>DD</sub> = 5.0V	80	40		ns
		V <sub>DD</sub> = 10V	40	20		ns
		V <sub>DD</sub> = 15V	20	10		ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Clock Rise and Fall Time	V <sub>DD</sub> = 5.0V	1			ms
		V <sub>DD</sub> = 10V	1			ms
		V <sub>DD</sub> = 15V	1			ms
t <sub>PC</sub>	Minimum Clock Pulse Width	V <sub>DD</sub> = 5.0V	200	100		ns
		V <sub>DD</sub> = 10V	100	50		ns
		V <sub>DD</sub> = 15V	83	40		ns
t <sub>PS</sub>	Minimum Strobe Pulse Width	V <sub>DD</sub> = 5.0V	200	100		ns
		V <sub>DD</sub> = 10V	80	40		ns
		V <sub>DD</sub> = 15V	70	35		ns
f <sub>max</sub>	Maximum Clock Frequency	V <sub>DD</sub> = 5.0V	1.5	3.0		MHz
		V <sub>DD</sub> = 10V	3.0	6.0		MHz
		V <sub>DD</sub> = 15V	4.0	8.0		MHz
C <sub>IN</sub>	Input Capacitance	Any Input		5.0	7.5	pF

**Note 5:** AC Parameters are guaranteed by DC correlated testing.

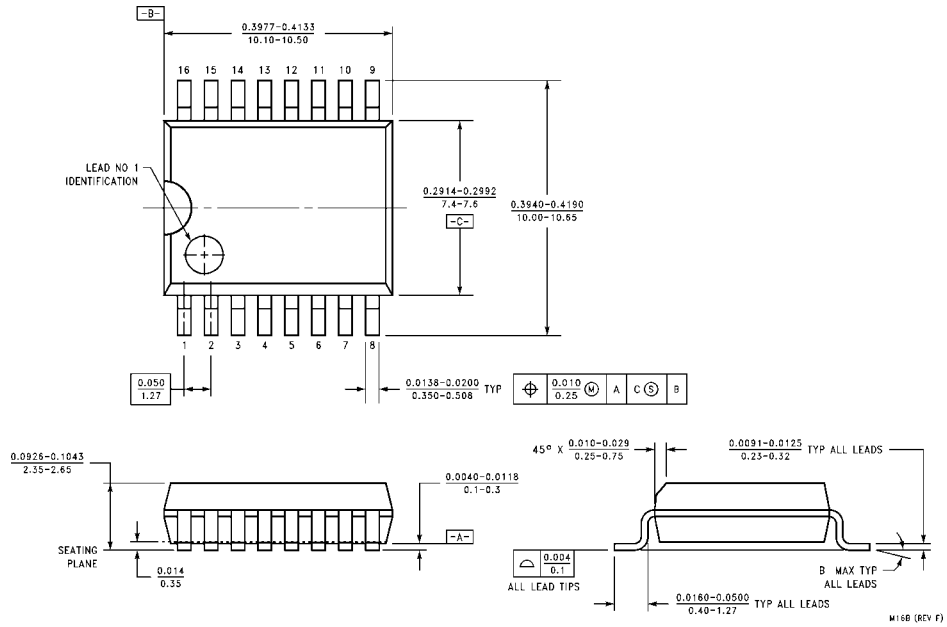
Timing Diagram



Test Circuits and Timing Diagrams for 3-STATE

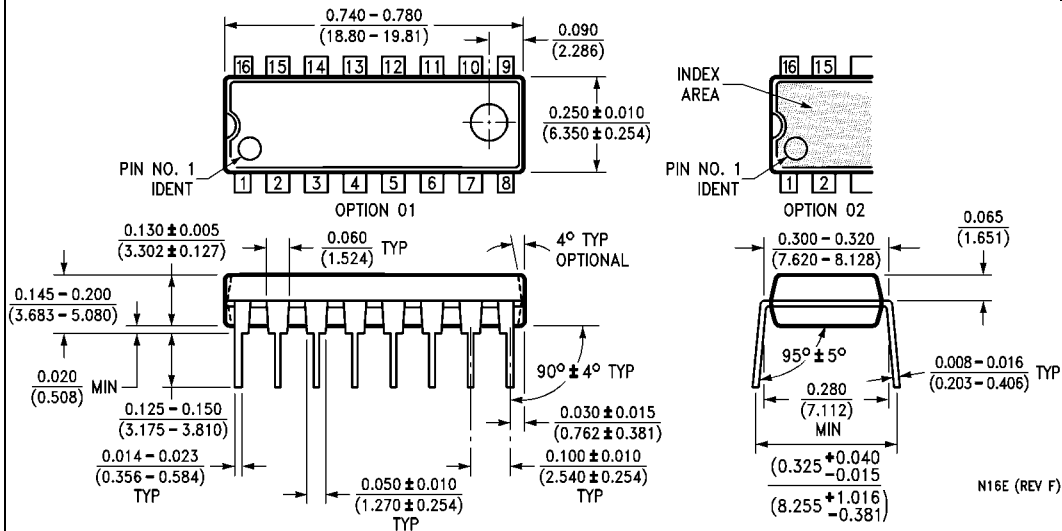


**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide M16B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N16E**

N16E (REV F)

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